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950 Rittenhouse Rd., Norristown, PA 19403 • Tel.: 215/666-7950 • TWX: 510/660-4168

65C23 TRI-PORT INTERFACE

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CONCEPT...

The 65C23 TRI-PORT Interface (TPI) is designed to simplify the implementation of complex I/O operations in microcomputer systems. It has three dedicated 8-bit I/O ports which provide 24 individually programmable I/O lines.

FEATURES:

- 24 individually programmable I/O lines
- Completely static operation
- Two TTL Drive Capability
- 6 directly addressable registers
- 1 MHz operation

65C23 Addressing

65C23 REGISTERS (Direct Addressing)

*000	R0	PRA — Port Register A
001	R1	PRB — Port Register B
010	R2	PRC — Port Register C
011	R3	DDRA — Data Direction Register A
100	R4	DDRB — Data Direction Register B
101	R5	DDRC — Data Direction Register C
*10		Illegal States
111		Illegal States

*NOTE: RS2, RS1, RS0 respectively

ORDER NUMBER:

MXS 65C23

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

65C23 PIN CONFIGURATION

VSS	1	40	DB7
PA0	2	39	DB6
PA1	3	38	DB5
PA2	4	37	DB4
PA3	5	36	DB3
PA4	6	35	DB2
PA5	7	34	DB1
PA6	8	33	DB0
PA7	9	32	PC7
PB0	10	31	PC6
PB1	11	30	PC5
PB2	12	29	PC4
PB3	13	28	PC3
PB4	14	27	PC2
PB5	15	26	PC1
PB6	16	25	PC0
PB7	17	24	RS0
CS	18	23	RS1
WRITE	19	22	RS2
VDD	20	21	RST

MOS Technology, Inc.
950 Rittenhouse Rd., Norristown, PA 19403
Tel.: 215/666-7950 TWX: 510/660-4186

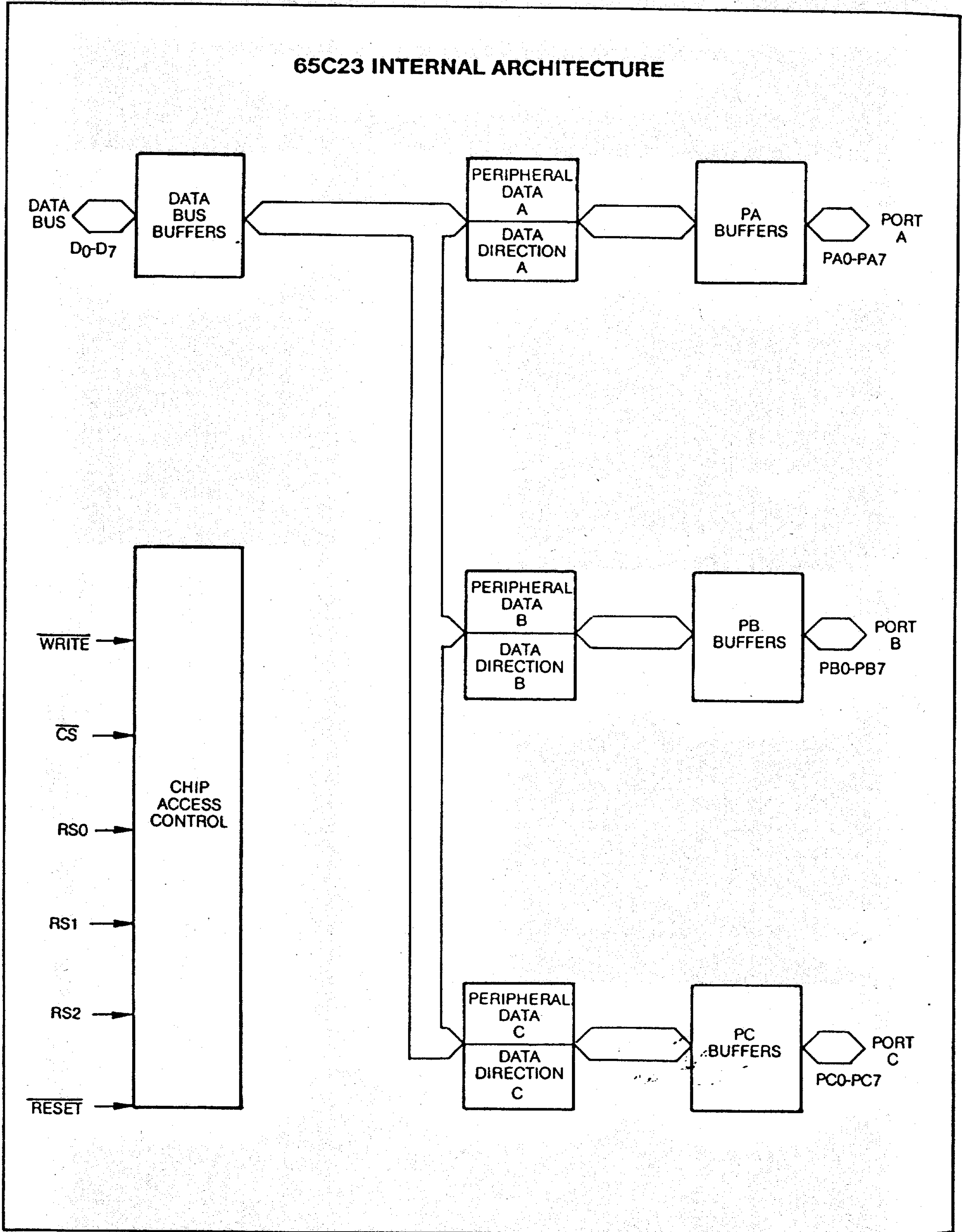
Frontier Manufacturing, Inc.
2955 N. Airway Ave., Costa Mesa, CA 92626
Tel.: 714/979-6300, TLX: 685649

commodore
semiconductor group

Optoelectronics, Inc.
4350 Beltwood Parkway South, Dallas, TX 75234
Tel: 214/387-0006 TLX 730969

Commodore Electronics Ltd.
Shing Dao Industrial Building
232 Aberdeen Main Rd., Hong Kong
Tel.: 5/540241, TLX: 78065366

65C23 INTERNAL ARCHITECTURE



MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	V_{CC}	-0.3 to +7.0	V _{dc}
INPUT VOLTAGE	V_{in}	-0.3 to +7.0	V _{dc}
OPERATING TEMPERATURE RANGE	T_A	0 to +70	°C
STORAGE TEMPERATURE RANGE	T_{stg}	-55 to +150	°C

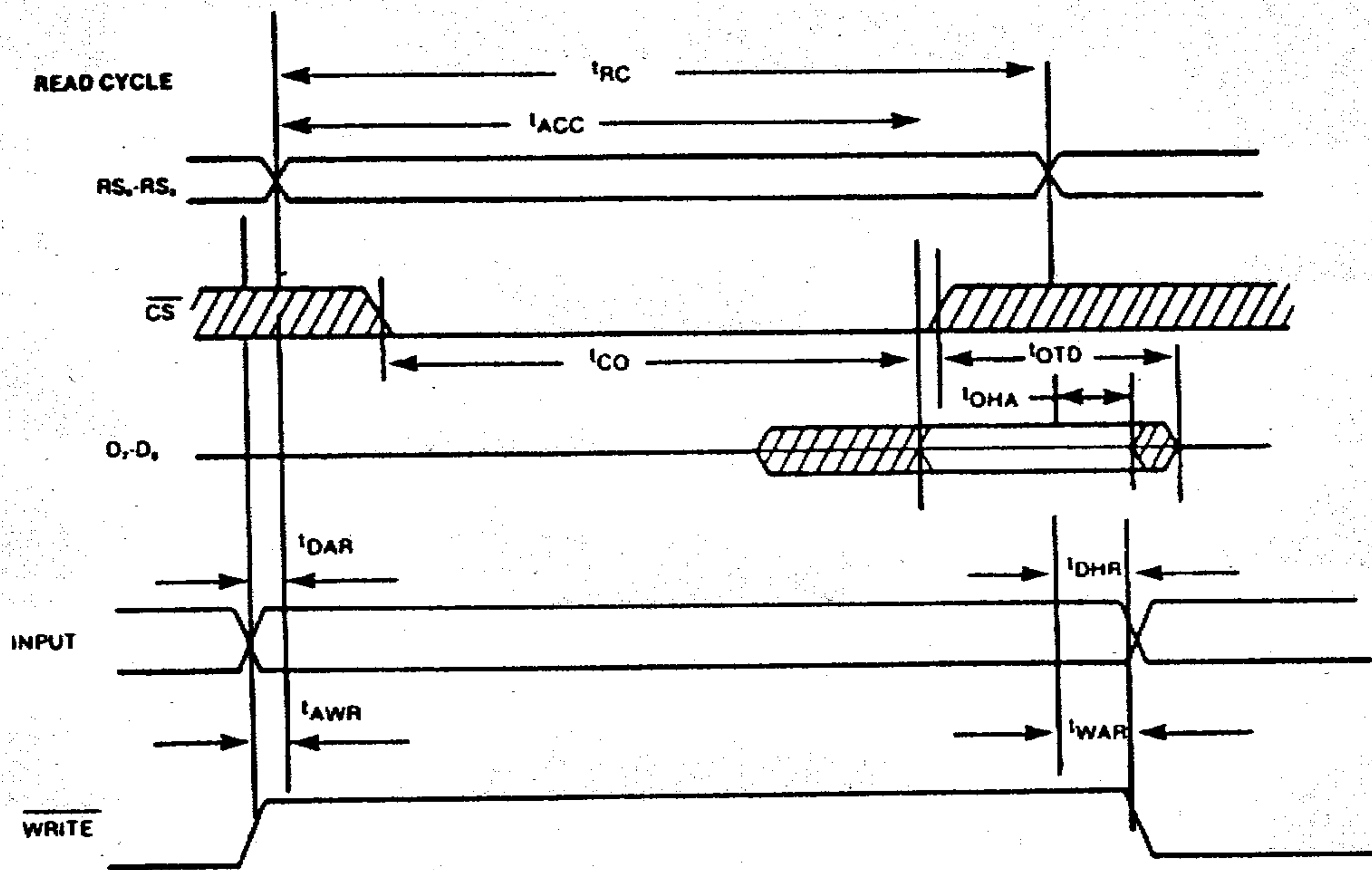
This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 5\%$, $V_{SS} = 0\text{V}$, $T_A = 0^\circ \text{ to } 70^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	—	V_{CC}	V _{dc}
Input Low Voltage (Normal Operating Levels)	V_{IL}	-0.3	—	+0.8	V _{dc}
Input Leakage Current $V_{in} = 0 \text{ to } 5.0 \text{ Vdc}$ WRITE \overline{RST} , \overline{CS} , \overline{RS} , $\overline{RS_2}$	I_{IN}	0	± 1.0	± 2.5	μAdc
Three-State (Off State) Input Current $(V_{in} = 0.4 \text{ to } 2.4 \text{ Vdc}, V_{CC} = \text{max})$ DO-D7, PA0-PA7, PB0-PB7, PC0-PC7	I_{TSI}	0	± 2.0	± 10	μAdc
Output High Voltage $(V_{CC} = \text{min}, \text{Load} = 200 \mu\text{Adc})$	V_{OH}	2.4	3.5	V_{CC}	V _{dc}
Output Low Voltage $(V_{CC} = \text{min}, \text{Load} = 3.2 \text{ mAdc})$	V_{OL}	V_{SS}	0.2	+0.4	V _{dc}
Output High Current (Sourcing) $(V_{OH} = 2.4 \text{ Vdc})$	I_{OH}	-200	-1000	—	μAdc
Output Low Current (Sinking) $(V_{OL} = 0.4 \text{ Vdc})$	I_{OL}	32	—	—	mAdc
Supply Current	I_{CC}	—	—	10	mA
Input Capacitance $(V_{in} = 0\text{V}, T_A = 25^\circ\text{C}, f = 1.0 \text{ MHz})$ DO-D7, PA0-PA7, PB0-PB7, PC0-PC7 WRITE \overline{RST} , $\overline{RS_0}$ - $\overline{RS_2}$, \overline{CS}	C_{in}	—	7	10	pF
Output Capacitance $(V_{in} = 0, T_A = 25^\circ\text{C}, f = 1.0 \text{ MHz})$	C_{out}	—	7	10	pF

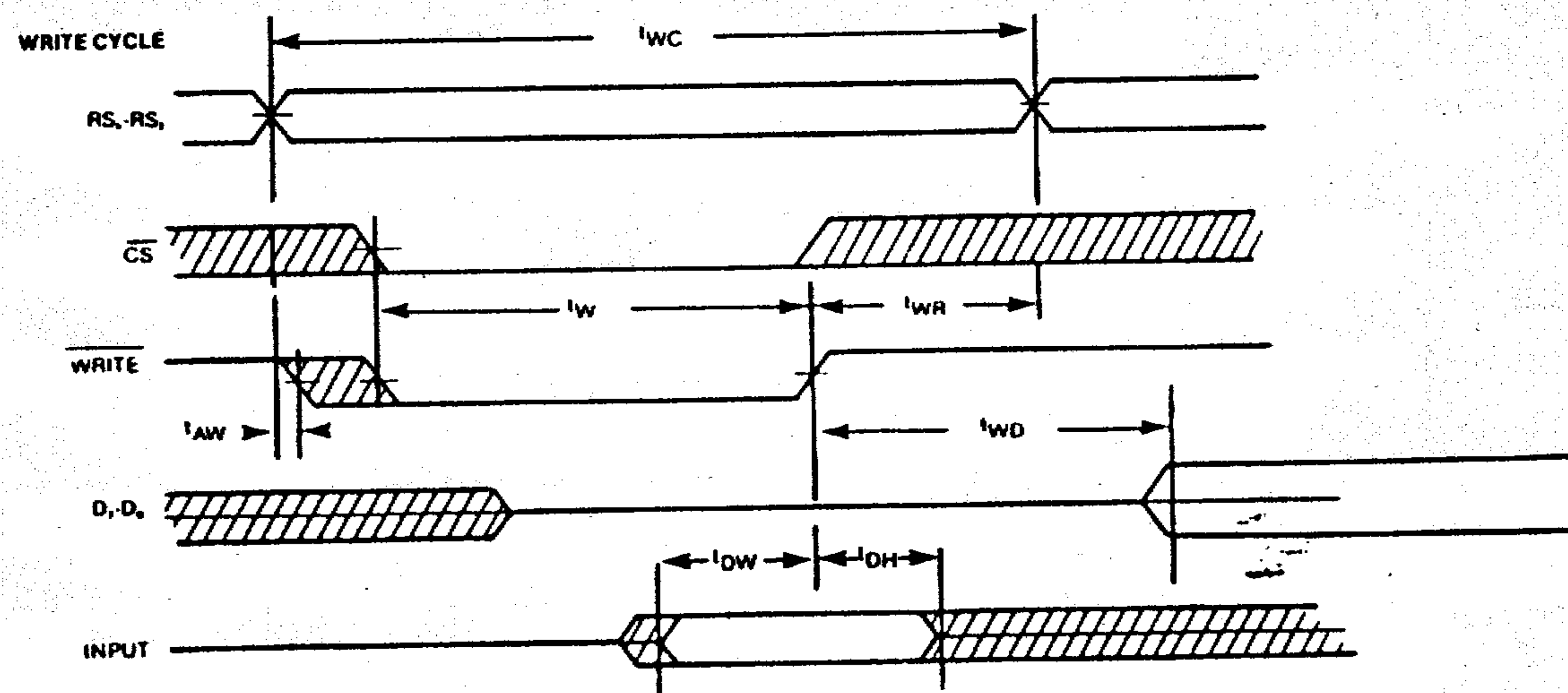
Note: Negative sign indicates outward current flow, positive indicates inward flow.

READ CYCLE



TIMING DIAGRAMS

WRITE CYCLE



READ CYCLE

Symbol	Parameter	MIN	MAX	UNITS
t _{RC}	Read Cycle Time	700		nS
t _{ACC}	Access time	450		nS
t _{CO}	Chip Select to Output Valid	450		nS
t _{OTD}	Chip Deselected to Output Off	0	100	nS
t _{OHA}	Output Hold From Address Change	50		nS
t _{DAR}	Peripheral Data Set-Up	120		nS
t _{DHR}	Peripheral Data Hold	0		nS
t _{AWR}	Write to Address Setup	0		nS
t _{WAR}	Write to Address Hold	0		nS

WRITE CYCLE

Symbol	Parameter	MIN	MAX	UNITS
t _{WC}	Write Cycle Time	700		nS
t _{AW}	Address to write set-up time	0		nS
t _W	Write Pulse Width	450		nS
t _{WR}	Write Release Time	250		nS
t _{DW}	Data to Write Overlap	150		nS
t _{DH}	Data Hold	50		nS
t _{WD}	Write to Peripheral Output	1000		nS

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