G65SCXX Series
G65SC1XX Series

CMD

Microcircuits

CMOS G65SCXXX 8-Bit Microprocessor Family

Features

- CMOS family that is compatible with NMOS 6500 series microprocessors
- Uses single +5 volt power supply
- Low power consumption (4mA @ 1 MHz) allows battery-powered operation
- Enhanced instruction set: 27 additional op codes encompassing eight new instructions enhance software performance compared to existing NMOS 6500 microprocessor instruction set
  —64 microprocessors instuctions
  —178 operational codes
  —15 addressing modes
- 65K-byte addressable memory
- 1, 2, 3, 4, 5 or 6 MHz operation
- Choice of external or on-board clock generator operation
- On-board clock generator/oscillator can be driven by an external single-phase clock input, an RC network, or a crystal circuit
- Advanced memory access timing ($\phi 4$) on selected versions
- Early address valid allows use with slower memories
- Early write data for dynamic memories
- 8-bit parallel processing
- Decimal and binary arithmetic
- Pipeline architecture
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- 8-bit bidirectional data bus
- "Ready" input (for single cycle execution)
- Direct memory access capability
- Bus compatible with M6800
- Available on selected versions, a memory lock output and bus enable input signals simplify multiprocessor designs

General Description

The G65SCXXX 8-bit microprocessor family is manufactured using the state-of-the-art silicon gate CMOS process. The G65SC02 and G65SC12 devices are pin-to-pin compatible with NMOS versions of the 6500 currently on the market. The G65SC102 and G65SC112 devices include several enhancements not available with other designs. All of the microprocessors are software compatible and provide 65K bytes of memory addressing and two interrupt inputs. All are bus compatible with MC6800 products.

As shown in Table I, the G65SC02, G65SC102 and G65SC112 clock generator circuit may be driven by an external crystal (Figure 2a), an RC network (Figure 2b) or by an external clock source. The G65SC12 requires an external clock source and is intended for multiprocessor applications where maximum timing control is necessary. The three family members with on-chip oscillators are intended for high performance, low cost operations where single phase inputs, crystals, or RC inputs provide the time base.

All of the microprocessors in the G65SCXXX family are pin-to-pin compatible with the NMOS 6500 microprocessors offered by several other manufacturers. However, the use of the leading-edge CMOS process technology ensures several software or programming enhancements not available to users fo the NMOS 6500. The enhancements include two additional addressing modes, an expanded microprocessor instruction set (from 56 to 64 instructions), and expanded operational codes (from 151 to 178). In addition, a series of operational enhancements are provided which materially improve the effective use of the microprocessor. These enhancements are explained in Table V of the section of this data sheet devoted to system software and programming. This series of microprocessors provides the user an architecture and instruction set with which he is basically familiar (6502), the several operational enhancements notwithstanding, plus all of the advantages of leading edge CMOS technology; i.e., increased noise immunity, higher reliability, and greatly reduced power consumption.

Table I. G65SCXXX Family Microprocessor Capabilities

ITEM NO.	PART NUMBER	DIP PINS	ADDRESSABLE MEMORY (BYTES)	ON-BOARD CLOCK OSCILLATOR (SEE NOTE)	EXTERNAL CLOCK GENERATOR REQUIRED	ADVANCED MEMORY ACCESS ($\phi 4$)	$\overline{IRQ}$	$\overline{NMI}$	$\overline{SO}$	DBE	BE	SYNC	RDY	$\overline{ML}$	$\overline{RES}$
1	G65SC02	40	65K	•			•	•	•			•	•		•
2	G65SC12	40	65K		•		•	•	•	•		•			•
3	G65SC102	40	65K	•		•	•	•	•		•	•	•	•	•
4	G65SC112	40	65K	•			•	•	•		•	•	•	•	•

NOTE: These devices can operate in any of the following clock generation modes 1 External crystal 2 External RC network 3 $\phi 0$(IN) from external clock source

General Description (Continued)

In addition to enhanced software programming, the use of CMOS processing also allows several hardware enhancements that are not available to users of the NMOS 6500 products. These hardware enhancements are listed and explained in Table II.
The G65SC102 offers the advantage of an on-board divide-by-four oscillator, increasing the available access time (tACC) by approximately 25%. All versions of the G65SCXXX microprocessor family are available in plastic, ceramic, cerdip, or leadless chip carrier packaging. All versions are available in 1, 2, 3, 4, 5 and 6 MHz maximum operating frequencies.

Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_S	-55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may result in permanent damage. Functional operation under these conditions is not implied.

DC Characteristics: V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T_A = −40°C to +85°C Industrial, 0° to +70°C Commercial

Parameter	Symbol	Min	Max	Unit
Input High Voltage φ0(IN), CLK (IN) φ2 (IN) $\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, $\overline{SO}$, DBE, BE	V_{IH}	 2.4 V_{DD}−0.2 2.0	 V_{DD}+0.3 V_{DD}+0.3 V_{DD}+0.3	 V V V
Input Low voltage φ0, (IN), CLK (IN) φ1 (IN) $\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, $\overline{SO}$, DBE, BE	V_{IL}	 −0.3 −0.3 −0.3	 0.4 0.2 0.8	 V V V
Input Leakage Current (V_{IN} = 0 to V_{DD}) $\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, $\overline{SO}$, DBE, BE (Internal Pull-Up). CLK (IN) [102] φ2 (IN), φ0 (IN), CLK (IN) [02, 12, 112]	I_{IN}		 1.0/−100 ±1.0	 μA μA
Three-State Leakage Current Address, Data, R/$\overline{W}$	I_{TSI}		±10.0	μA
Output High Voltage (I_{OH} = −100 μA, V_{DD} = 4.75V) SYNC, Data, A0–A15, R/$\overline{W}$	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 1.6 mA, V_{DD} = 4.5V) SYNC, Data, A0–A15, R/$\overline{W}$	V_{OL}	—	0.4	V
Supply Current f = 1 MHz (No Load) f = 2 MHz f = 3 MHz f = 4 MHz	I_{DD}	—	4 8 12 16	mA
Standby Power Dissipation (φ2 = V_{IH}, Inputs = V_{SS} or V_{DD} Outputs Unloaded)	P_{SBY}		50.0	μW
Capacitance (V_{IN} = 0, T_A = 25°C, f = 1 MHz Logic, φ0(IN), CLK (IN) A0–A15, R/$\overline{W}$ Data (Three-State) φ2 (IN)	 C_{IN} C_{TS} C2(IN)	 — — —	 10 15 40	pF

AC Characteristics, G65SC02, G65SC12, G65SC112: V_{DD} = 5.0V ± 5%. T_A = −40° C to +85° Industrial.
0° C to +70°C Commercial

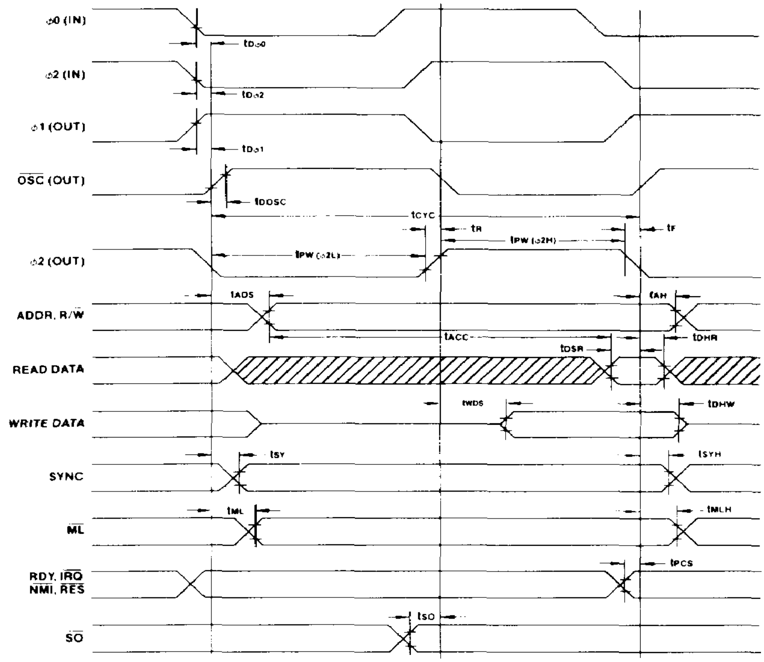
		1 MHz		2 MHz		3 MHz		4 MHz		5 MHz		6 MHz		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Delay Time, ϕ0 (IN) to ϕ2 (OUT)	$t_{D\phi 0}$	—	40	—	40	—	40	—	40	—	35	—	30	nS
Delay Time, ϕ2 (IN) to ϕ2 (OUT)	$t_{D\phi 2}$	—	35	—	35	—	35	—	35	—	35	—	30	nS
Delay Time, ϕ1 (OUT) to ϕ2 (OUT)	$t_{D\phi 1}$	—	50	—	50	—	50	—	50	—	35	—	30	NS
Delay Time, ϕ2 (OUT) to $\overline{OSC}$ (OUT)	t_{DOSC}	—	50	—	50	—	50	—	50	—	35	—	30	nS
Cycle Time	t_{CYC}	1.0	DC	0.50	DC	0.33	DC	0.25	DC	0.20	DC	0.167	DC	μS
Clock Pulse Width Low	t_{PW} (ϕ2L)	430	10000	210	10000	150	10000	100	10000	90	10000	80	10000	nS
Clock Pulse Width High	t_{PW} (ϕ2H)	450	—	220	—	160	—	110	—	85	—	75	—	nS
Fall Time, Rise Time	t_F, t_R	—	25	—	20	—	15	—	12	—	10	—	10	nS
Address Hold Time	t_{AH}	15	—	15	—	15	—	15	—	5	—	5	—	nS
Address Setup Time	t_{ADS}	—	125	—	100	—	85	—	70	—	60	—	55	nS
Access Time	t_{ACC}	775	—	340	—	200	—	140	—	110	—	85	—	nS
Read Data Hold Time	t_{DHR}	10	—	10	—	10	—	10	—	5	—	5	—	nS
Read Data Setup Time	t_{DSR}	100	—	60	—	40	—	30	—	27	—	25	—	nS
Write Data Delay Time	t_{WDS}	—	175	—	100	—	75	—	55	—	50	—	45	nS
Write Data Hold Time	t_{DHW}	30	—	30	—	30	—	30	—	15	—	15	—	nS
SYNC, $\overline{ML}$ Setup Time	t_{SY}, t_{ML}	—	125	—	100	—	85	—	70	—	60	—	55	nS
SYNC, $\overline{ML}$ Hold Time	t_{SYH}, T_{MLH}	10	—	10	—	10	—	10	—	5	—	5	—	nS
$\overline{SO}$ Setup Time	t_{SO}	75	—	50	—	35	—	25	—	22	—	20	—	nS
Processor Control Setup Time	t_{PSC}	200	—	110	—	80	—	60	—	55	—	50	—	nS

AC Characteristics, G65SC102: V_{DD} = 5.0V ±5%. T_A = −40° C to ±85° C Industrial, 0° C to ±70° C Commercial

		1 MHz		2 MHz		3 MHz		4 MHz		5 MHz		6 MHz		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Delay Time, CLK (IN) to ϕ2 (OUT)	t_{CLK}	—	75	—	75	—	75	—	75	—	60	—	50	nS
Delay Time, $\overline{OSC}$ (OUT) to ϕ2 (OUT)	t_{DOSC}	—	70	—	70	—	70	—	70	—	55	—	45	n
Cycle Time	t_{CYC}	1.0	DC	0.50	DC	0.33	DC	0.25	DC	0.20	DC	0.167	DC	μS
Clock Pulse Width Low	t_{PW} (ϕ2L)	430	10000	210	10000	150	10000	100	10000	90	10000	80	10000	nS
Clock Pulse Width High	t_{PW} (ϕ2H)	450	—	220	—	160	—	110	—	85	—	75	—	nS
Fall Time, Rise Time	t_F, t_R	—	25	—	20	—	15	—	12	—	10	—	10	nS
Delay Time, ϕ2 (OUT) to ϕ4 (OUT)	t_{AVS}	—	250	—	125	—	83	—	63	—	52	—	42	nS
Address Valid to ϕ4 (OUT)	$t_{A\phi 4}$	100	—	25	—	16	—	12	—	8	—	5	—	nS
Address Hold Time	t_{AH}	15	—	15	—	15	—	15	—	10	—	10	—	nS
Access Time	t_{ACC}	775	—	340	—	200	—	140	—	110	—	85	—	nS
Read Data Hold Time	t_{DHR}	10	—	10	—	10	—	10	—	5	—	5	—	nS
Read Data Setup Time	t_{DSR}	100	—	60	—	40	—	30	—	27	—	25	—	nS
Write Data Hold Time	t_{DHW}	30	—	30	—	30	—	30	—	15	—	15	—	nS
Write Data Delay Time	$t_{DD\phi 4}$	—	200	—	110	—	85	—	65	—	50	—	45	nS
SYNC, $\overline{ML}$ Setup Time	t_{SY}, t_{ML}	—	125	—	100	—	85	—	70	—	60	—	55	nS
SYNC, $\overline{ML}$ Hold Time	t_{SYH}, t_{MLH}	10	—	10	—	10	—	10	—	5	—	5	—	nS
$\overline{SO}$ Setup Time	t_{SO}	75	—	50	—	35	—	25	—	22	—	20	—	nS
Processor Control Setup Time	t_{PCS}	200	—	110	—	80	—	80	—	55	—	50	—	nS

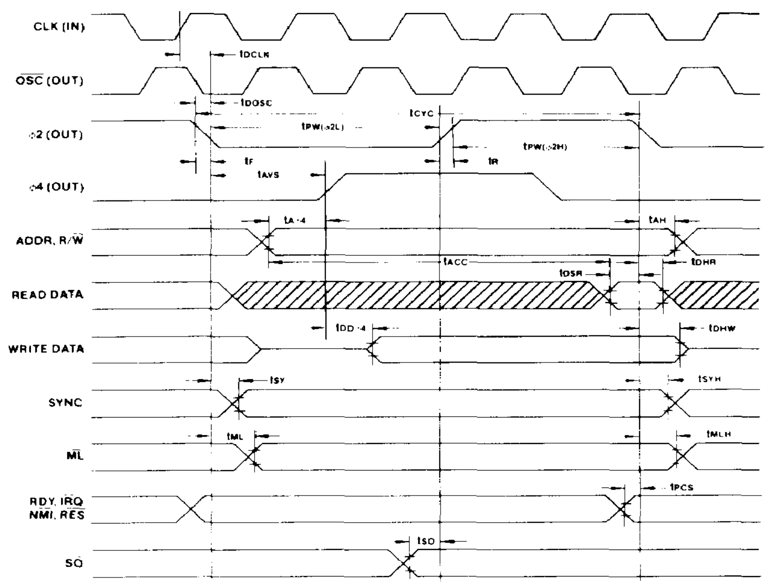
TIMING DIAGRAM:

G65SC02
G65SC12
G65SC112

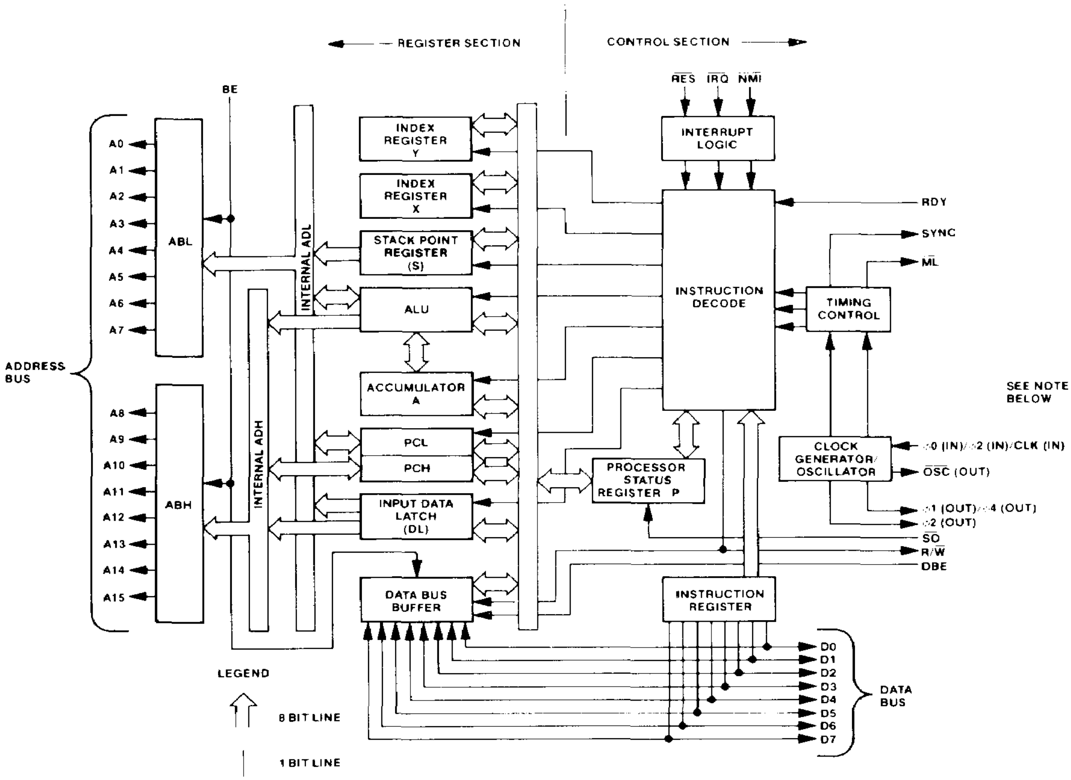


TIMING DIAGRAM:

G65SC102



Notes
1. Load = 100 pF.
2. Voltage levels shown are V_L = 0.4 V, V_H = 2.4 V, unless otherwise specified.
3. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.



Note: Refer to Table I for signal input/output applicability.

Figure 1. Internal Architecture Simplified Block Diagram

Functional Description

Timing Control

The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase one clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

Program Counter

The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

Instruction Register and Decode

Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

Arithmetic and Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations

Functional Description (Continued)

Index Registers

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible.

Stack Pointer

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{NMI}$ and $\overline{IRQ}$). The stack allows simple implementation of nested subroutines and multiple level interrupts.

Processor Status Register

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The 6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

Signal Description

Address Bus (AO-AXX)

Refer to the particular package configuration for the respective number of address lines.

In both the 40-pin and 44-pin packages, A0-A15 forms a 16-bit address bus for memory and I/O exchanges on the data bus. The address lines are set (See BE below.) to the high impedance state by the bus enable (BE) signal. The output of each address line is TTL compatible, capable of driving one standard TTL load and 130 pF.

Bus Enable (BE)

This signal allows external control of the data and the address output buffers and R/$\overline{W}$. For normal operation, BE is high causing the address buffers and R/$\overline{W}$ to be active and the data buffers to be active during a write cycle. For external control, BE is held low to disable the buffers.

Clock In (CLK (IN))

The 65SC10X Series is supplied with an internal clock generator operating at four times the $\phi 2$ frequency. The frequency of these clocks is externally controlled by the crystal or oscillator circuit shown in Figure 2.

Phase 0 In (ϕ0(IN))

This is the buffered clock input to the internal clock generator on the G65SC0X series. Clock outputs ϕ1(OUT) and ϕ2(OUT) are derived from this signal.

Phase 2 In (ϕ2(IN))

This is the unbuffered clock input to the internal clock generator on the G65SC1X and G65SC11X series. The clock output, ϕ2(OUT), is derived from this signal.

Data Bus Enable (DBE)

This TTL-compatible input allows external control of the three-state data output buffers. In normal operation, DBE would be driven by the phase two (ϕ2) clock, thus allowing data input from microprocessor only during ϕ2. During the read cycle, the data bus buffers are internally disabled, becoming essentially an open circuit. To disable the data bus externally, DBE should be held low.

Data Bus (D0-D7)

The data lines (D0-D7) constitute an 8-bit bidirectional data bus used for data exchanges to and from the device and peripherals. The outputs are three-state buffers capable of driving one TTL load and 130 pF. The data lines are set to the high impedance state by BE or DBE.

Interrupt Request ($\overline{IRQ}$)

This TTL compatible signal requests that an interrupt sequence begin within the microprocessor. The $\overline{IRQ}$ is sampled during ϕ2 operation; if the interrupt flag in the processor status register is zero, the current instruction is completed and the interrupt sequence begins during ϕ1. The program counter and processor status register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3K ohm external resistor should be used for proper wire-OR operation.

Memory Lock ($\overline{ML}$)

In a multiprocessor system, $\overline{ML}$ indicates the need to defer the rearbitration of the next bus cycle to ensure the integrity of read-modify-write instructions. $\overline{ML}$ goes low during ASL, DEC, INC, LSR, ROL, ROR, TRB, TSB memory referencing instructions. This signal is low for the modify and write cycles.

Non-Maskable Interrupt ($\overline{NMI}$)

A negative-going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. The $\overline{NMI}$ is sampled during ϕ2; the current instruction is completed and the interrupt sequence begins during ϕ1. The program counter is loaded with the interrupt vector from locations FFFA (low byte) and FFFB (high byte), thereby transferring program control to the non-maskable interrupt routine. However, it should be noted this is an edge-sensitive input. As a result, another interrupt will occur if there is another negative-going transition and the program has not returned from a previous interrupt. Also, no interrupt will occur if $\overline{NMI}$ is low and negative-going edge has not occurred since the last non-maskable interrupt.

Oscillator Out ($\overline{OSC}$ (OUT))

On the G65SC102 microprocessor, an internal inverter and a resistor are connected between pins 35 and 37 on the DIP package and pins 39 and 41 on the PLCC package. The inverter has sufficient loop gain to provide oscillation using an external crystal.

Phase 1 Out (ϕ1(OUT))

This inverted ϕ2(OUT) signal provides timing for external R/$\overline{W}$ operations.

Phase 2 Out (ϕ2(OUT))

This signal provides timing for external bus R/$\overline{W}$ operations. Addresses are valid after the address setup time (t_{ADS}) from the falling edge of ϕ2(OUT).

Phase 4 Out (ϕ4(OUT))

This signal is delayed by t_{AVS} from ϕ2(OUT). The address output is valid prior to the rising edge of ϕ4(OUT).

Signal Description (Continued)

Ready (RDY)
This input signal allows the user to single-cycle the microprocessor on all cycles including write cycles. A negative transition to the low state during or coincident with phase one (ϕ1) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two (ϕ2) in which the ready signal is low. This feature allows microprocessor interfacing with low-speed memory as well as direct memory access (DMA).

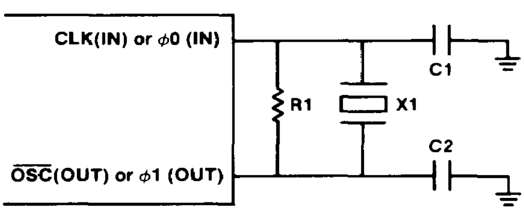
Reset ($\overline{\text{RES}}$)
This input is used to reset the microprocessor. Reset must be held low for at least two clock cycles after V_{DD} reaches operating voltage from a power down. A positive transition on this pin will then cause an initialization sequence to begin. After the system has been operating, a low on this line of at least two cycles will cease microprocessing activity.

When a positive edge is detected, there is an initialization sequence lasting six clock cycles. The previous program counter and status register values are written to the stack memory area. Then the interrupt mask flag is set, the decimal mode is cleared and the program counter is loaded with the restart vector from locations FFFC (low byte) and FFFD (high byte). This is the start location for program control. This input should be high in normal operation.

Read/Write (R/$\overline{\text{W}}$)
This signal is normally in the high state indicating that the microprocessor is reading data from memory or I/O bus. In the low state the data bus has valid data from the microprocessor to be stored at the addressed memory location. R/$\overline{\text{W}}$ is set to the high impedance state by BE.

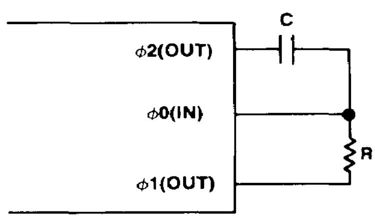
Set Overflow ($\overline{\text{SO}}$)
A negative transition on this line sets the overflow bit in the status code register. The signal is sampled on the trailing edge of ϕ1.

Synchronize (SYNC)
This output line is provided to identify those cycles during which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during ϕ1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.



C1, C2 = 51pF
R1 = 200KΩ (not required for G65SC102)
X1 = 1MHz

Figure 2(a). Crystal Circuit for Internal Oscillator



Suggested RC network configuration for internal oscillator.

1 MHz operation at V_{DD} = 5.0V:
C = 56pF
R = 5.6 KΩ

Figure 2(b). RC Circuit for Internal Oscillator

Table II. Microprocessor Hardware Enhancements

Function	NMOS 6500	G65SCXXX Family
Oscillator.	Requires external active components.	Crystal or RC network will oscillate when connected between ϕ0 (IN) and ϕ1 (OUT).
Assertion of Ready (RDY) during write operations.	Ignored.	Stops processor during ϕ2.
1X series clock inputs.	Two non-overlapping clock inputs (ϕ1 and ϕ2) are required.	ϕ2 (IN) is the only required clock.
Unused input-only pins ($\overline{\text{IRQ}}$, $\overline{\text{NMI}}$, RDY, $\overline{\text{RES}}$, $\overline{\text{SO}}$, DBE, BE).	Must be connected to low impedance signal to avoid noise problems.	Connected internally by a high-resistance to V_{DD} (approximately 1 Megohm).

Addressing Modes

Fifteen addressing modes are available to the user of the GTE G65SCXXX family of microprocessors. The addressing modes are described in the following paragraphs:

Implied Addressing
In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

Accumulator Addressing
This form of addressing is represented with a one byte instruction and implies an operation on the accumulator.

Immediate Addressing
With immediate addressing, the operand is contained in the second byte of the instruction; no further memory addressing is required.

Absolute Addressing
For absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Therefore, this addressing mode allows access to the total 65K bytes of addressable memory.

Zero Page Addressing
Zero page addressing allows shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. The careful use of zero page addressing can result in significant increase in code efficiency.

Absolute Indexed Addressing
Absolute indexed addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X and Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

Zero Page Indexed Addressing
Zero page absolute addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order eight bits of memory and crossing of page boundaries does not occur.

Relative Addressing
Relative addressing is used only with branch instruction; it establishes a destination for the conditional branch.

Zero Page Indexed Indirect Addressing
With zero page indexed indirect addressing (usually referred to as Indirect X) the second byte of the instruction is added to the contents of the X index register; the carry is discarded. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

Absolute Indexed Indirect Addressing (Jump Instruction Only)
With absolute indexed indirect addressing, the contents of the second and third instruction bytes are added to the X register. The result of this addition points to a memory location containing the lower-order eight bits of the effective address. The next memory location contains the higher-order eight bits of the effective address.

Indirect Indexed Addressing
This form of addressing is usually referred to as Indirect, Y. The second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

Zero Page Indirect Addressing
In this form of addressing, the second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits is always zero. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address.

Absolute Indirect Addressing (Jump Instruction Only)
The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the 16 bits of the program counter.

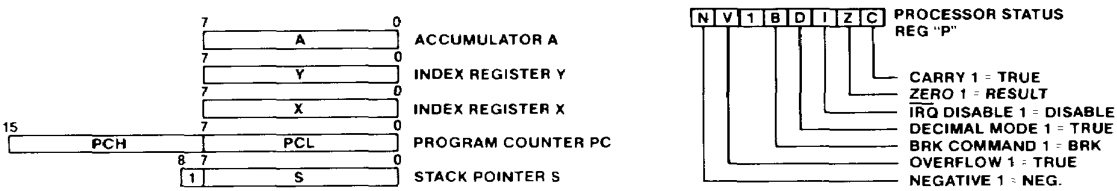


Figure 3. Microprocessor Programming Model

Table III. Instruction Set—Alphabetical Sequence

	ADC	Add Memory to Accumulator with Carry
	AND	"AND" Memory with Accumulator
	ASL	Shift One Bit Left
	BCC	Branch on Carry Clear
	BCS	Branch on Carry Set
	BEQ	Branch on Result Zero
	BIT	Test Memory Bits with Accumulator
	BMI	Branch on Result Minus
	BNE	Branch on Result Not Zero
	BPL	Branch on Result Plus
●	BRA	Branch Always
	BRK	Force Break
	BVC	Branch on Overflow Clear
	BVS	Branch on Overflow Set
	CLC	Clear Carry Flag
	CLD	Clear Decimal Mode
	CLI	Clear Interrupt Disable Bit
	CLV	Clear Overflow Flag
	CMP	Compare Memory and Accumulator
	CPX	Compare Memory and Index X
	CPY	Compare Memory and Index Y
	DEC	Decrement by One
	DEX	Decrement Index X by One
	DEY	Decrement Index Y by One
	EOR	"Exclusive-or" Memory with Accumulator
	INC	Increment by One
	INX	Increment Index X by One
	INY	Increment Index Y by One
	JMP	Jump to New Location
	JSR	Jump to New Location Saving Return Address
	LDA	Load Accumulator with Memory
	LDX	Load Index X with Memory
	LDY	Load Index Y with Memory
	LSR	Shift One Bit Right
	NOP	No Operation
	ORA	"OR" Memory with Accumulator
	PHA	Push Accumulator on Stack
	PHP	Push Processor Status on Stack
●	PHX	Push Index X on Stack
●	PHY	Push Index Y on Stack
	PLA	Pull Accumulator from Stack
	PLP	Pull Processor Status from Stack
●	PLX	Pull Index X from Stack
●	PLY	Pull Index Y from Stack
	ROL	Rotate One Bit Left
	ROR	Rotate One Bit Right
	RTI	Return from Interrupt
	RTS	Return from Subroutine
	SBC	Subtract Memory from Accumulator with Borrow
	SEC	Set Carry Flag
	SED	Set Decimal Mode
	SEI	Set Interrupt Disable Bit
	STA	Store Accumulator in Memory
	STX	Store Index X in Memory
	STY	Store Index Y in Memory
●	STZ	Store Zero in Memory
	TAX	Transfer Accumulator to Index X
	TAY	Transfer Accumulator to Index Y
●	TRB	Test and Reset Memory Bits with Accumulator
●	TSB	Test and Set Memory Bits with Accumulator
	TSX	Transfer Stack Pointer to Index X
	TXA	Transfer Index X to Accumulator
	TXS	Transfer Index X to Stack Pointer
	TYA	Transfer Index Y to Accumulator

Note ● · New Instruction

MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	BRK	ORA ind, X			TSB zpg	ORA zpg	ASL zpg		PHP	ORA imm	ASL A		TSB abs	ORA abs	ASL abs		0
1	BPL rel	ORA ind, Y	ORA ind		TRB zpg	ORA zpg, X	ASL zpg, X		CLC	ORA abs, Y	INC A		TRB abs	ORA abs, X	ASL abs, X		1
2	JSR abs	AND ind, X			BIT zpg	AND zpg	ROL zpg		PLP	AND imm	ROL A		BIT abs	AND abs	ROL abs		2
3	BMI rel	AND ind, Y	AND ind		BIT zpg, X	AND zpg, X	ROL zpg, X		SEC	AND abs, Y	DEC A		BIT abs, X	AND abs, X	ROL abs, X		3
4	RTI	EOR ind, X				EOR zpg	LSR zpg		PHA	EOR imm	LSR A		JMP abs	EOR abs	LSR abs		4
5	BVC rel	EOR ind, Y	EOR ind			EOR zpg, X	LSR zpg, X		CLI	EOR abs, Y	PHY			EOR abs, X	LSR abs, X		5
6	RTS	ADC ind, X			STZ zpg	ADC zpg	ROR zpg		PLA	ADC imm	ROR A		JMP ind	ADC abs	ROR abs		6
7	BVS rel	ADC ind, Y	ADC ind		STZ zpg, X	ADC zpg, X	ROR zpg, X		SEI	ADC abs, Y	PLY		JMP ind, X	ADC abs, X	ROR abs, X		7
8	BRA rel	STA ind, X			STY zpg	STA zpg	STX zpg		DEY	BIT imm	TXA		STY abs	STA abs	STX abs		8
9	BCC rel	STA ind, Y	STA ind		STY zpg, X	STA zpg, X	STX zpg, Y		TYA	STA abs, Y	TXS		STZ abs	STA abs, X	STZ abs, X		9
A	LDY imm	LDA ind, X	LDX imm		LDY zpg	LDA zpg	LDX zpg		TAY	LDA imm	TAX		LDY abs	LDA abs	LDX abs		A
B	BCS rel	LDA ind, Y	LDA ind		LDY zpg, X	LDA zpg, X	LDX zpg, Y		CLV	LDA abs, Y	TSX		LDY abs, X	LDA abs, X	LDX abs, Y		B
C	CPY imm	CMP ind, X			CPY zpg	CMP zpg	DEC zpg		INY	CMP imm	DEX		CPY abs	CMP abs	DEC abs		C
D	BNE rel	CMP ind, Y	CMP ind			CMP zpg, X	DEC zpg, X		CLD	CMP abs, Y	PHX			CMP abs, X	DEC abs, X		D
E	CPX imm	SBC ind, X			CPX zpg	SBC zpg	INC zpg		INX	SBC imm	NOP		CPX abs	SBC abs	INC abs		E
F	BEQ rel	SBC ind, Y	SBC ind			SBC zpg, X	INC zpg, X		SED	SBC abs, Y	PLX			SBC abs, X	INC abs, X		F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

Note ▭ = New Op Codes

Figure 4. Microprocessor Op Code Table

Table IV. Operational Codes, Execution Time, and Memory Requirements

MNEMONIC	OPERATION	IMMEDIATE			ABSOLUTE			ZERO PAGE			(4) IMPLIED			(IND, X)			(1) (IND), Y			ZPG,X			(1) ABS,X			(1) ABS,Y			RELATIVE (2)			INDIRECT			ZPG,Y			PROCESSOR STATUS CODE 7 6 4 3 2 1 0	MNEMONIC
		OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N V B D I Z C	
ADC	A + M + C → A (3)	69	2	2	6D	4	3	65	3	2				61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3				72	5	2				N V • • • Z C	ADC
AND	A∧M → A	29	2	2	2D	4	3	25	3	2				21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3				32	5	2				N • • • • Z •	AND
ASL	C ← [7 0] ← 0				0E	6	3	06	5	2	0A	2	1							16	6	2	1E	6	3													N • • • • Z C	ASL
BCC	BRANCH IF C=0																												90	2	2							• • • • • • •	BCC
BCS	BRANCH IF C=1																												B0	2	2							• • • • • • •	BCS
BEQ	BRANCH IF Z=1																												F0	2	2							• • • • • • •	BEQ
BIT	A∧M (5)	89	2	2	2C	4	3	24	3	2										34	4	2	3C	4	3													M₇ M₆ • • • Z •	BIT
BMI	BRANCH IF N=1																												30	2	2							• • • • • • •	BMI
BNE	BRANCH IF Z=0																												D0	2	2							• • • • • • •	BNE
BPL	BRANCH IF N=0																												10	2	2							• • • • • • •	BPL
BRA	BRANCH ALWAYS																												80	2	2							• • • • • • •	BRA
BRK	BREAK										00	7	1																									• • 1 0 1 • •	BRK
BVC	BRANCH IF V=0																												50	2	2							• • • • • • •	BVC
BVS	BRANCH IF V=1																												70	2	2							• • • • • • •	BVS
CLC	0 → C										18	2	1																									• • • • • • 0	CLC
CLD	0 → D										D8	2	1																									• • • 0 • • •	CLD
CLI	0 → I										58	2	1																									• • • • 0 • •	CLI
CLV	0 → V										B8	2	1																									• 0 • • • • •	CLV
CMP	A-M	C9	2	2	CD	4	3	C5	3	2				C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3				D2	5	2				N • • • • Z C	CMP
CPX	X-M	E0	2	2	EC	4	3	E4	3	2																												N • • • • Z C	CPX
CPY	Y-M	C0	2	2	CC	4	3	C4	3	2																												N • • • • Z C	CPY
DEC	DECREMENT				CE	6	3	C6	5	2	3A	2	1							D6	6	2	DE	6	3													N • • • • Z •	DEC
DEX	X-1 → X										CA	2	1																									N • • • • Z •	DEX
DEY	Y-1 → Y										88	2	1																									N • • • • Z •	DEY
EOR	A∀M → A	49	2	2	4D	4	3	45	3	2				41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3				52	5	2				N • • • • Z •	EOR
INC	INCREMENT				EE	6	3	E6	5	2	1A	2	1							F6	6	2	FE	6	3													N • • • • Z •	INC
INX	X + 1 → X										E8	2	1																									N • • • • Z •	INX
INY	Y + 1 → Y										C8	2	1																									N • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3							7C	6	3																6C	6	3				• • • • • • •	JMP
JSR	JUMP SUB				20	6	3																															• • • • • • •	JSR
LDA	M → A	A9	2	2	AD	4	3	A5	3	2				A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3				B2	5	2				N • • • • Z •	LDA
LDX	M → X	A2	2	2	AE	4	3	A6	3	2																BE	4	3							B6	4	2	N • • • • Z •	LDX
LDY	M → Y	A0	2	2	AC	4	3	A4	3	2										B4	4	2	BC	4	3													N • • • • Z •	LDY
LSR	0 → [7 0] → C				4E	6	3	46	5	2	4A	2	1							56	6	2	5E	6	3													0 • • • • Z C	LSR
NOP	NO OPERATION										EA	2	1																									• • • • • • •	NOP
ORA	AVM → A	09	2	2	0D	4	3	05	3	2				01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3				12	5	2				N • • • • Z •	ORA
PHA	A → Ms S-1 → S										48	3	1																									• • • • • • •	PHA
PHP	P → Ms S-1 → S										08	3	1																									• • • • • • •	PHP
PHX	X → Ms S-1 → S										DA	3	1																									• • • • • • •	PHX
PHY	Y → Ms S-1 → S										5A	3	1																									• • • • • • •	PHY
PLA	S+1 → S Ms → A										68	4	1																									N • • • • Z •	PLA
PLP	S+1 → S Ms → P										28	4	1																									N V 1 D I Z C	PLP
PLX	S+1 → S Ms → X										FA	4	1																									N • • • • Z •	PLX
PLY	S+1 → S Ms → Y										7A	4	1																									N • • • • Z •	PLY
ROL	← [7 0] ← C ←				2E	6	3	26	5	2	2A	2	1							36	6	2	3E	6	3													N • • • • Z C	ROL
ROR	→ C → [7 0] →				6E	6	3	66	5	2	6A	2	1							76	6	2	7E	6	3													N • • • • Z C	ROR
RTI	RTRN INT										40	6	1																									N V 1 D I Z C	RTI
RTS	RTRN SUB										60	6	1																									• • • • • • •	RTS
SBC	A-M-C̄ → A (3)	E9	2	2	ED	4	3	E5	3	2				E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3				F2	5	2				N V • • • Z C	SBC
SEC	1 → C										38	2	1																									• • • • • • 1	SEC
SED	1 → D										F8	2	1																									• • • 1 • • •	SED
SEI	1 → I										78	2	1																									• • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2				81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3				92	5	2				• • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																									96	4	2	• • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2										94	4	2																• • • • • • •	STY
STZ	00 → M				9C	4	3	64	3	2										74	4	2	9E	5	3													• • • • • • •	STZ
TAX	A → X										AA	2	1																									N • • • • Z •	TAX
TAY	A → Y										A8	2	1																									N • • • • Z •	TAY
TRB	Ā∧M → M (6)				1C	6	3	14	5	2																												• • • • • Z •	TRB
TSB	AVM → M (6)				0C	6	3	04	5	2																												• • • • • Z •	TSB
TSX	S → X										BA	2	1																									N • • • • Z •	TSX
TXA	X → A										8A	2	1																									N • • • • Z •	TXA
TXS	X → S										9A	2	1																									• • • • • • •	TXS
TYA	Y → A										98	2	1																									N • • • • Z •	TYA

Notes

1. Add 1 to "n" if page boundary is crossed, except STA and STZ
2. Add 1 to "n" if branch occurs to same page. Add 2 to "n" if branch occurs to different page.
3. Add 1 to "n" if decimal mode.
4. Accumulator address is included in Implied address
5. "N" and "V" flags are unchanged in immediate mode
6. Z flag indicates AAM result (same as BIT instruction)

X Index X
Y Index Y
A Accumulator
M Memory per effective address
Ms *Memory per stack pointer*

\+ Add
− Subtract
∧ And
V Or
∀ *Exclusive or*

n No. Cycles
\# No. Bytes
M_6 Memory Bit #6
M_7 Memory Bit #7

Enhanced Operational Characteristics

The CMD G65SCXXX family of microprocessors is a complete series of devices designed for building state-of-the-art microcomputer systems. Each member of the family is carefully designed to be hardware compatible, utilize the same basic software instruction set, and to be bus compatible with the MC6800 product line. Accordingly, the G65SCXX series is pin compatible with existing NMOS 6500 type microprocessors.

However, as stated previously, the CMOS design allows several operational enhancements to be incorporated in the current product. These operational enhancementse are explained in Table V.

Table V. Microprocessor Operational Enhancements

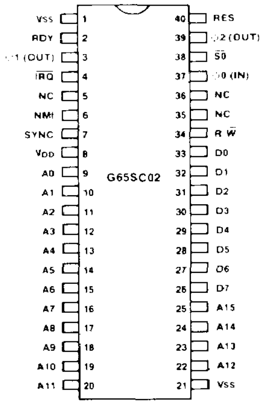
Function	NMOS 6500 Microprocessor	G65SCXXX Family Microprocessor
Indexed addressing across page boundary.	Extra read of invalid address.	Extra read of last instruction byte.
Execution of invalid op codes.	Some terminate only by reset. Results are undefined.	All are NOPs (reserved for future use). Op Code / Bytes / Cycles X2 / 2 / 2 X3, X7, XB, XF / 1 / 1 44 / 2 / 3 54, D4, F4 / 2 / 4 5C / 3 / 8 DC, FC / 3 / 4
Jump indirect, operand = XXFF.	Page address does not increment.	Page address increments, one additional cycle.
Read/modify/write instructions at effective address.	One read and two write cycles.	Two read and one write cycle.
Decimal flag.	*Indeterminate after reset.*	*Initialized to binary mode (D=0) after reset and interrupts.*
Flags after decimal operation.	Invalid N, V and Z flags.	Valid flags. One additional cycle.
Interrupt after fetch of BRK instruction.	Interrupt vector is loaded; BRK vector is ignored.	BRK is executed, then interrupt is executed.
Reset	Reads three stack locations.	Writes program counter and status register to stack
Read/Modify/Write instructions absolute indexed in same page.	Seven cycles.	Six cycles.

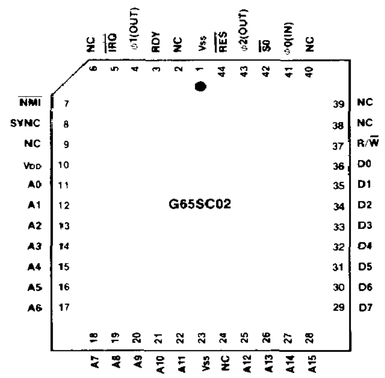
Pin Function

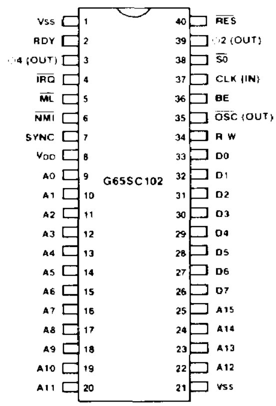
Pin	Description
A0–Axx	Address Bus
BE	Bus Enable
CLK (IN)	Clock Input
φ0(IN)	Phase 0 In
φ2(IN)	Phase 2 In
DBE	Data Bus Enable
D0–D7	Data Bus
$\overline{IRQ}$	Interrupt Request
$\overline{ML}$	Memory Lock
NC	No Connection
$\overline{NMI}$	Non-Maskable Interrupt

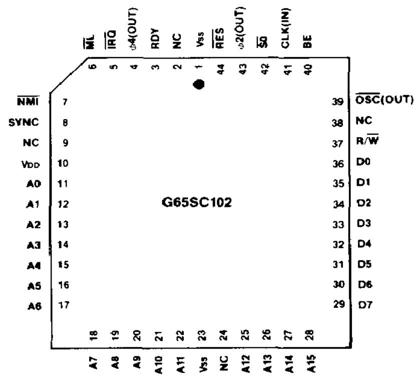
Pin	Description
$\overline{OSC}$ (OUT)	Oscillator Output
φ1(OUT)	Phase 1 Out
φ2(OUT)	Phase 2 Out
φ4(OUT)	Phase 4 Out
RDY	Ready
$\overline{RES}$	Reset
R/$\overline{W}$	Read/Write
$\overline{SO}$	Set Overflow
SYNC	Synchronize
V_{DD}	Positive Power Supply (+5.0 Volts)
V_{SS}	Internal Logic Ground

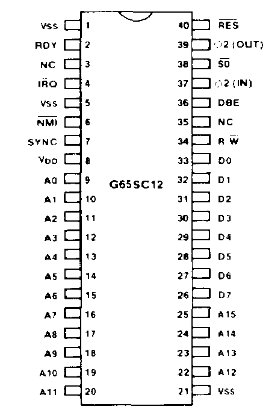
Pin Configuration

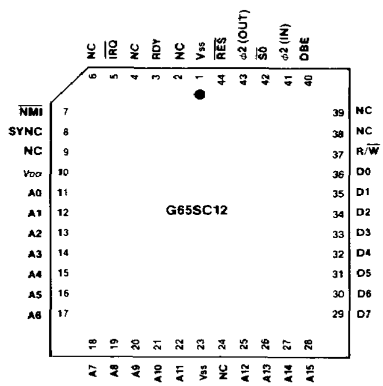




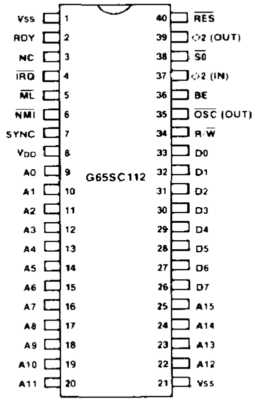


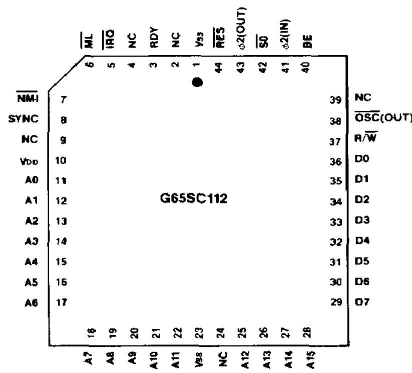






Pin Configuration, Continued





Ordering Information

G 65SCXXX A P I -2

Description
C—Special G—Standard

Product Identification Number

Version

Package

P—Plastic E—Leaded Chip Carrier
C—Ceramic L—Leadless Chip Carrier
D—Cerdip X—Dice

Temperature/Processing

None— 0°C to +70°C, ± 5% P.S. Tol. S— 0°C to +70°C, ± 10% P.S. Tol.
I— -40°C to +85°C, ± 5% P.S. Tol. W— -40°C to +85°C, ± 10% P.S. Tol.

Performance Designator

Designators selected for speed and power specifications

-1 1MHz -3 3MHz -5 5MHz
-2 2MHz -4 4MHz -6 6MHz